REMARKS/ARGUMENT

Claim 32 has been amended better to define the claimed invention and overcome the 35 U.S.C. 112, second paragraph rejection.

1) Claims 1-3, 12, 20, 21, 24 and 25 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kenington (U.S. 6,794,931). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1-3, 12, 20, 21, 24 and 25 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California,* 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.,* 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1, as amended, requires and positively recites, an **integrated transceiver** circuit, comprising: "a digital polar transmitter path that provides an amplitude/phase signal from a digital input, the transmitter path including at least one digital predistorter that predistorts the digital input to mitigate nonlinearities associated with a power amplifier", "a **receiver path associated with the digital transmitter path**", "a coupling element that provides the signal from the transmitter path to the receiver path" and "a signal evaluator that determines values for at least one parameter associated with the digital predistorter based on the signal".

Independent Claim 21 requires and positively recites, a method of calibrating a predistortion component in **a transceiver system**, comprising: "providing a first digital signal, containing amplitude information related to a desired analog signal, to a transmitter path", "providing a second digital signal, containing phase information related to the desired analog signal, to the transmitter path", "predistorting at least one of the first digital signal and the second digital signal in the digital domain according to at least one predistortion parameter", "generating an analog signal from the first digital signal and the second digital signal" and "processing the analog signal at **a receiver path associated with the transmitter path** to determine values for the at least one predistortion parameter".

Independent Claim 24 requires and positively recites, an **integrated transceiver circuit**, comprising: "means for producing a digital input", "means for predistorting the digital input to mitigate nonlinear error associated with a power amplifier according to one or more predistortion parameters", "**means for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain**", "means for generating an analog signal from the digital input" and "means for analyzing the analog signal to determine appropriate predistortion parameters for the means for predistorting".

In contrast, Kensington does not teach or suggest "an **integrated transceiver** circuit" as required by Claims 1 and 24 OR "**a transceiver system**", as required by Claim 21. Kensington does not teach "a receiver path associated with the digital transmitter path", as suggested by Examiner. The circuit pointed out by Examiner ("comprising (712)" in Figure 7) (page 3 of OA) is not the associated receiver as defined by the "transceiver" association. It is merely a sensor that is incapable of taking on any "receiver path" roles.

In addition, the examiner is incorrect in stating that "Kensington discloses an integrated transceiver circuit" (page 3 of OA). The receiver part of the transceiver is missing. As such, Kensington fails to teach or suggest, "an **integrated transceiver** circuit" and "a **receiver path**

associated with the digital transmitter path", as required by Claim 1 OR "**a transceiver system**" and "processing the analog signal at **a receiver path associated with the transmitter path** to determine values for the at least one predistortion parameter", as required by Claim 21, OR "an **integrated transceiver** circuit" and "**means for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain**", as required by Claim 24. Accordingly, the 35 U.S.C. 102(e) rejection of Claims 1, 21 and 24 is improper and must be withdrawn.

Claims 2-3, 12 and 20 stand allowable as depending directly, or indirectly, respectively from allowable Claim 1. Claim 25 stands allowable for depending from Claim 24.

Claim 2 further defines the circuit of claim 1, the transmitter path comprising a gain normalization component that transfers the digital input **from a normalized domain** to a domain that is dependent on process, voltage, and temperature (PVT) variations. Claim 2 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1. Moreover, Examiner states on page 3, "Kensington discloses that transmitter path comprises a process component (comprising (D/A, VCO), (considered here equivalent with the limitation "gain normalization component"), that transfers the digital input from a digitized signal domain, (considered here equivalent with the limitation "normalized domain", to a phase domain that is dependent on voltage variations inputted to (VCO) to generate a phase-modulated RF output of (VCO)". Examiner is incorrect in equating the digitized signal domain in Kensington with the normalized domain, as required by Claim 2. There is no such connection since "digitized" does not implied "normalized". This is a consequence of incorrectly equating "process components", D/A and VCO, in Kensington with the gain normalization component of Claim 2. For example, there are two gain normalization components revealed in the specification of the present application: 26 & 34 (Figure 1), 114 & 124 (Figure 2), and 214 & 224 (Figure 3) of the frequency and amplitude paths, respectively. Their inputs "all operate within a normalized domain, such that the inputs and outputs of the components are normalized to standard system parameters (e.g., a reference voltage or an outermost circle on an I/Q

constellation)" [0018]. Also, "the gain normalization component 34 can adjust for changes in the temperature and voltage experienced by the system components" [0018]. There is no such teaching or suggestion in Kensington. For example, if the gain of VCO in Kensington (commonly designated as KVCO in the units of Hz/V) changes due to temperature, there is no normalization adjustment performed. Accordingly, the 35 U.S.C. 102(e) rejection of Claim 2 is improper and must be withdrawn.

Claim 3 further defines the circuit of claim 2, the digital predistorter preceding the gain **normalization component** on the transmitter path, such that the digital predistorter predistorts the digital input **in the normalized domain**. Claim 3 depends from Claim 2 and stands allowable for the same reasons set forth above in support of the allowability of Claim 2. Moreover, for the additional reasons set forth above in support of Claim 2, the rejection is improper. Again, Kensington does not teach the "normalized domain" as required by Claim 3. The predistorter 316 or 718 on Figure 7 of Kensington certainly does not "predistort … in the normalized domain". Accordingly, the 35 U.S.C. 102(e) rejection of Claim 3 is improper and must be withdrawn.

Claim 12 further defines the circuit of claim 1, the power amplifier comprising an external power amplifier that is external to the integrated transceiver circuit. Claim 12 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 20 further defines the circuit of claim 1, the transmitter path being **operative to alternate between a saturation mode, in which the power amplifier is driven at saturation, and a linear mode, in which the power amplifier operates within a linear range**. Claim 20 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1. Moreover, Examiner is incorrect in stating that alternating between a saturation mode and a linear mode is equivalent to linearizing a non-linear amplifier. While it is a goal of linearizing a non-linear amplifier by virtue of predistortion, it is not possible to

linearize an amplifier that already operates in saturation. Saturated-mode amplifiers are typically driven by regulating their power supply voltage, which is a technique well known in the art. The reference of McCune, which was brought up by Examiner further explains it. Accordingly, the 35 U.S.C. 102(e) rejection of Claim 20 is improper and must be withdrawn.

Claim 25 further defines the circuit of claim 24, the means for generating the analog signal comprising means for synthesizing a radio frequency signal from a digital input. Claim 25 depends from Claim 24 and stands allowable for the same reasons set forth above in support of the allowability of Claim 24.

2) Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by McCune et al. (U.S. 6,366,177). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1 and 12 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California,* 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.,* 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1, as amended, requires and positively recites, an **integrated transceiver** circuit, comprising: "a digital polar transmitter path that provides an amplitude/phase signal from a digital input, the transmitter path including at least one digital

predistorter that predistorts the digital input to mitigate nonlinearities associated with a power amplifier", "a **receiver path associated with the digital transmitter path**", "a coupling element that provides the signal from the transmitter path to the receiver path" and "a signal evaluator that determines values for at least one parameter associated with the digital predistorter based on the signal".

In contrast, McCune does not teach or suggest "an **integrated transceiver** circuit" as required by Claim 1. McCune similarly does not teach "a receiver path associated with the digital transmitter path", as suggested by Examiner. The circuit pointed out by Examiner ("1031, 1033 and 1011 is not the receiver. As such, McCune fails to teach or suggest, "an **integrated transceiver** circuit" and "a **receiver path associated with the digital transmitter path**", as required by Claim 1. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 1 is improper and must be withdrawn.

Claim 12 further defines the circuit of claim 1, the power amplifier comprising an external power amplifier that is external to the integrated transceiver circuit. Claim 12 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

3) Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kensington (U.S. 6,794,931). Applicants respectfully traverse this rejection, as set forth below.

Claim 4 further defines the circuit of claim 1, the power amplifier comprising an internal power amplifier that is integrated into the integrated transceiver circuit, the **power amplifier accepting digital RF input**. Claim 4 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1. Moreover, the power amplifier in Kensington clearly does not accept a digital RF input, as required by Claim 4. It is impermissible for Examiner to equate the switch labeled "High-Speed RF Switch" to the internal

power amplifier, which is labeled in Kensington as "Non-linear RF Amplifier". The switch is just a passing switch without any amplification or generation properties. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 4 is improper and must be withdrawn.

Claim 5 further defines the circuit of claim 4, the internal power amplifier comprising a **Class E** switching amplifier. Claim 5 depends from Claim 4 and stands allowable for the same reasons set forth above in support of the allowability of Claim 4. Moreover, the class E switching amplifier is coupled to the "digital RF input" of Claim 4. One cannot have a class E switching amplifier without a digital RF input. The power amplifier (Non-linear RF Amplifier, sometimes labeled 216) in Figures 2—9 in Kensington cannot possibly operate in class E mode due to the existence of the High-Speed RF Switch. The stated class E amplifier in Background is not related to the invention in Kensington and is only for completeness. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 5 is improper and must be withdrawn.

4) Claims 1, 12, 13, 14, 15, 16, 18, 21, 22, 24 and 25 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Camp, Jr et al (6,191,653). Applicants respectfully traverse this rejection, as set forth below.

Independent Claim 1, as amended, requires and positively recites, an **integrated transceiver** circuit, comprising: "a digital polar transmitter path that provides an amplitude/phase signal from a digital input, the transmitter path including at least one digital predistorter that predistorts the digital input to mitigate nonlinearities associated with a power amplifier", "a **receiver path associated with the digital transmitter path**", "a coupling element that provides the signal from the transmitter path to the receiver path" and "a signal evaluator that determines values for at least one parameter associated with the digital predistorter based on the signal".

Independent Claim 21 requires and positively recites, a method of calibrating a predistortion component in **a transceiver system**, comprising: "providing a first digital signal, containing amplitude information related to a desired analog signal, to a transmitter path", "providing a second digital signal, containing phase information related to the desired analog signal, to the transmitter path", "predistorting at least one of the first digital signal and the second digital signal in the digital domain according to at least one predistortion parameter", "generating an analog signal from the first digital signal and the second digital signal" and "processing the analog signal at **a receiver path associated with the transmitter path** to determine values for the at least one predistortion parameter".

Independent Claim 24 requires and positively recites, an **integrated transceiver circuit**, comprising: "means for producing a digital input", "means for predistorting the digital input to mitigate nonlinear error associated with a power amplifier according to one or more predistortion parameters", "**means for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain**", "means for generating an analog signal from the digital input" and "means for analyzing the analog signal to determine appropriate predistortion parameters for the means for predistorting".

In contrast, Camp does not teach or suggest "an **integrated transceiver** circuit" as required by Claims 1 and 24 OR "**a transceiver system**", as required by Claim 21. Camp does not teach "a receiver path associated with the digital transmitter path (see figure 5, col. 3, line 8 to col. 4, line 38, col. 6, line 28 to col. 7, line 12)", as suggested by Examiner. The circuit pointed out by Examiner is not the "receiver" of the "integrated transceiver", as required by Claims 1, 21 and 24. It is rather a control loop system of the output power: "The power level at the output of the power amplifier 32 is measured with a power detector circuit 42" (column 4, lines 20-22 is part of the same text cited by Examiner). As such, Camp fails to teach or suggest, "an **integrated transceiver** circuit" as required by Claims 1 and 24 OR "**a transceiver system**", as required by Claim 21. Accordingly, the 35 U.S.C. 102(e) rejection of Claims 1, 21 and 24 is improper and must be withdrawn.

Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Moreover, even had the Examiner considered all of the words of Claims 1, 21 and 24, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification**. *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious**. *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985). For the reasons set forth above, Examiner has not set forth a prima facie case of obviousness for Claims 1, 21 and 24. Accordingly, the 35 U.S.C. 103(a) rejection of Claims 1, 21 and 24 is improper and must be withdrawn.

Claims 12-16 and 18 stand allowable as depending directly, or indirectly, respectively

from allowable Claim 1. Claim 22 stands allowable for depending from Claim 21. Claim 25 stands allowable for depending from Claim 24.

Claim 12 further defines the circuit of claim 1, the power amplifier comprising an external power amplifier that is external to the integrated transceiver circuit. Claim 12 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 13 further defines the circuit of claim 12, the power amplifier further comprising an internal power amplifier, the output of the internal power amplifier being provided to the external power amplifier. Claim 13 depends from Claim 12 and stands allowable for the same reasons set forth above in support of the allowability of Claim 12.

Claim 14 further defines the circuit of claim 12, the digital transmitter path comprising an amplitude modulated path that controls the supply to the external amplifier according to a first digital input, and a phase modulated path that provides a radio frequency input to the external power amplifier according to a second digital input. Claim 14 depends from Claim 12 and stands allowable for the same reasons set forth above in support of the allowability of Claim 12.

Claim 15 further defines the circuit of claim 14, the phase modulated path comprising a **digitally controlled oscillator**. Claim 15 depends from Claim 14 and stands allowable for the same reasons set forth above in support of the allowability of Claim 14. Moreover, VCO 452 in Camp is a voltage controlled oscillator (VCO) – NOT a digitally controlled oscillator, as determined by Examiner.

Claim 16 further defines the circuit of claim 15, the phase modulated path comprising a gain normalization component that **adjusts the second digital input for process, voltage and temperature (PVT) variations associated with the digitally controlled oscillator**. Claim 16 depends from Claim 15 and stands allowable for the same reasons set forth above in support of

the allowability of Claim 15. Moreover, Camp does NOT teach that "process component (470, 452, 458, 456, 450)" serves the same role as gain normalization component for the digitally controlled oscillator, as determined by Examiner. Camp actually teaches that "the level and phase of the second path match the level and phase of the first path so that the frequency response of the composite paths is flat". The gains of the modulation paths is a cascade of gains of various components along the way of each path (e.g., VCO, D/A; and Phase Detector and Loop Filter). As such, it is not possible to isolate VCO (equated by the examiner to DCO) gain. At best, the cascaded gains of several components of one path can be matched to the cascaded gain of another set of components of the second path. This is what is taught in Figure 5 in Camp. There is no possibility or even motivation to "**adjusts … for process, voltage and temperature (PVT) variations associated with the digitally controlled oscillator**", as required by Claim 16. Another consequence of the above considerations is that the voltage and temperature variations, being dynamic in nature cannot be adjusted, especially in the field. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 16 is improper and must be withdrawn.

Claim 18 further defines the circuit of claim 14, the amplitude modulated path comprising a digital predistorter that adjusts the first digital input to mitigate nonlinearities associated with the power amplifier. Claim 18 depends from Claim 14 and stands allowable for the same reasons set forth above in support of the allowability of Claim 14.

Claim 22 further defines the method of claim 21, further comprising **converting the first digital signal and the second digital signal from associated normalized domains to process, voltage, and temperature (PVT) dependent domains**. Moreover, Camp does NOT teach that "process component (470, 452, 458, 456, 450)" serves the same role as gain normalization component for the digitally controlled oscillator, as determined by Examiner. Camp actually teaches that "the level and phase of the second path match the level and phase of the first path so that the frequency response of the composite paths is fiat". The gains of the modulation paths is a cascade of gains of various components along the way of each path (e.g., VCO, D/A; and Phase Detector and Loop Filter). As such, it is not possible to isolate VCO (equated by the

examiner to DCO) gain. At best, the cascaded gains of several components of one path can be matched to the cascaded gain of another set of components of the second path. This is what is taught in Figure 5 in Camp. In addition, the "second digital signal" (i.e., phase) does not get compensated for the variations in PVT of the PA and associated circuitry. Contrary to the examiner's contention (with lack of specific references given -- the inventors would appreciate the examiner pointing it out.), there is no "normalized domain" of the first signal.

There is no possibility or even motivation to "**converting the first digital signal and the second digital signal from associated normalized domains to process, voltage, and temperature (PVT) dependent domains**", as required by Claim 22. Another consequence of the above considerations is that the voltage and temperature variations, being dynamic in nature cannot be adjusted, especially in the field. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 22 is improper and must be withdrawn.

Claim 25 further defines the circuit of claim 24, the means for generating the analog signal comprising means for synthesizing a radio frequency signal from a digital input. Claim 25 depends from Claim 24 and stands allowable for the same reasons set forth above in support of the allowability of Claim 24.

5) Claims 14 and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Camp, Jr et al (6,191,653). Applicants respectfully traverse this rejection, as set forth below.

Claim 14 further defines the circuit of claim 12, the digital transmitter path comprising an amplitude modulated path that controls the supply to the external amplifier according to a first digital input, and a phase modulated path that provides a radio frequency input to the external power amplifier according to a second digital input. Claim 14 depends from Claim 12 and therefore stands allowable for the same reasons set forth above in support of the allowance of Claims 1 and 12 over McCune.

Claim 17 further defines the circuit of claim 14, the phase modulated path comprising a digital predistorter that adjusts the second digital input to mitigate nonlinearities associated with the power amplifier. Claim 17 depends from Claim 14 above and stands allowable for the same reasons set forth above.

Applicants appreciate Examiner's indication that Claims 6-11, 19, 23 and 26-31 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims however Applicants believe that for the reasons set forth above, Claims 6-11, 19, 23 and 26-31 are allowable in their current form.

Claims 1-32 stand allowable for the reasons set forth above. Applicants respectfully request withdrawal of the remaining rejections and allowance of the application at the earliest possible date.

Respectfully submitted,

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